IN THE CLAIMS:

1. (Original) A reset apparatus for a clocking subsystem of a data processing system having a clock source, comprising:

a phase locked loop (PLL) having a reference clock input for receiving clock signals from the clock source, a reset input for receiving a PLL reset signal that resets the PLL, the PLL further having an output that delivers phase aligned clock signals to logic of the data processing system;

a circuit having a clock input to receive the clock signals and a reset input to receive a circuit reset signal, the circuit further having a PLL reset output to deliver the PLL reset signal to the PLL;

a first timer having an input that receives the clock signals, the first timer generating a first timer signal in response to receiving the clock signals, and not generating the first timer signal in response to not receiving the clock signals; and

a second timer having an input to receive the first timer signal, an output to deliver the circuit reset signal to the circuit in response to detecting an absence of the first timer signal, the circuit rest signal causing the circuit to reset the PLL.

2. (Original) The apparatus of claim 1, further comprising:

the circuit having a global reset output for delivering global reset signals to logic of the data processing system.

3. (Original) The apparatus of claim 1, further comprising:

the first timer signal generated by the first timer is a pulsed signal, and the second timer is configured to detect the presence or absence of the pulsed signal at its input.

1   4. (Original) The apparatus of claim 1, further comprising:

2   the second timer is a watchdog timer that generates the circuit reset signal after a

3   delay period.

1   5. (Original) The apparatus of claim 1, further comprising:

2   the clock source is a processor of the data processing system and the clock signals

3   are forwarded clock signals.

1   6. (Original) The apparatus of claim 1, further comprising:

2   the circuit having an external reset input for receiving an external reset signal and

3   an error reset output for delivering an error reset signal to a set of error registers, the er-

4   ror registers storing information related to the cause of a system error, the error reset sig-

5   nal being asserted in response to assertion of the external reset signal.

1   7. (Original) The apparatus of Claim 6, further comprising:

2   the external reset signal is generated by a voltage monitor device in response to

3   power transitions.

1   8. (Currently amended) The apparatus as in claim 7, <u>wherein</u> ~~further comprising~~:

2   the <u>set of</u> error registers are control status registers<u>.</u>

1   9. (Original) The apparatus of claim 1, further comprising:

2   the second timer issuing the circuit reset signal to the circuit before clock signals

3   are received at the first timer; and,

4 the circuit asserting the PLL reset signal and a global reset signal in response to the

5 reset signal from the second timer.

1 10. (Original) The apparatus of claim 9, further comprising:

2   the second timer halting issuance of the circuit reset signal in response to receiv-

3 ing the first timer signal; and,

4   the circuit releasing the PLL reset signal after a predetermined period of time has

5 elapsed since receiving the circuit reset signal.

1 11. (Original) The apparatus of claim 10, further comprising:

2   the circuit, after a subsequent predetermined period of time has elapsed since re-

3 ceiving the circuit reset signal, releasing the global reset signal and distributing the phase-

4 aligned clock signals to logic of the data processing system.

1 12. (Original) A method for resetting a clocking subsystem of a data processing system,

2 the method comprising:

3   providing a phase locked loop (PLL) having a reference clock input for receiving

4 clock signals from a clock source, a reset input for receiving a PLL reset signal that resets

5 the PLL, the PLL further having an output that delivers phase aligned clock signals to

6 logic of the data processing system

7   providing a circuit having a clock input to receive the clock signals and a reset

8 input to receive a circuit reset signal, the circuit further having a PLL reset output to de-

9 liver the PLL reset signal to the PLL;

10   generating a first timer signal at a first timer circuit in response to receiving the

11 clock signals, and not generating the first timer signal in response to not receiving the

12 clock signals; and,

13   detecting the absence of the first timer signal at a second timer having an input to

14   receive the first timer signal, and in response to detecting the absence of the first timer

15   signal outputting the circuit reset signal to the circuit to enable the circuit to reset the PLL

16   in the absence of the clock signals.

1   13. (Original) The method of Claim 12, further comprising:

2   generating a global reset signal at the circuit, the circuit having a global reset sig-

3   nal output interconnected to logic of the data processing system.

1   14. (Original) The method of Claim 12, further comprising

2   generating the first timer signal as a pulsed signal, and the second timer is config-

3   ured to detect the presence or absence of the pulsed signal at its input.

1   15. (Original) The method of Claim 12, further comprising:

2   generating the circuit reset signal after a delay period.

1   16. (Original) The method of Claim 12, further comprising:

2   providing the clock signals are forwarded clock signals from a processor of the

3   data processing system.

1   17. (Original) The method of Claim 12, further comprising:

2   providing an external reset input at the circuit for receiving an external reset sig-

3   nal and providing an error reset output at the circuit for delivering an error reset signal to

4   a set of error registers; and,

5   asserting the error reset signal in response to assertion of the external reset signal.

1   18. (Original) The method of Claim 17, further comprising:

2   generating the external reset signal at a voltage monitor device in response to

3   power transitions.

1   19. (Currently amended) The method of Claim 18, wherein ~~further comprising~~:

2   ~~providing~~ the set of error registers are control status registers.

1   20. (Original) The method of claim 12, further comprising:

2   issuing the circuit reset signal from the second timer to the circuit before clock

3   signals are received at the first timer; and,

4   asserting the PLL reset signal and a global reset signal at the circuit in response to

5   the reset signal from the second timer.

1   21. (Original) The method of claim 20, further comprising:

2   halting issuance of the circuit reset signal at the second timer in response to re-

3   ceiving the first timer signal at the second timer; and,

4   releasing the PLL reset signal at the circuit after a predetermined period of time

5   has elapsed since receiving the circuit reset signal.

1   22. (Original) The method of claim 20, further comprising:

2   after a subsequent predetermined period of time has elapsed since receiving the

3   circuit reset signal, releasing the global reset signal at the circuit and distributing the

4   phase-aligned clock signals to logic of the data processing system.

1   23. (Currently amended) A reset apparatus for a clocking subsystem of a data processing

2   system having a clock source, comprising:

3   means for delivering phase aligned clock signals from a phase locked loop (PLL)

4   to logic of the data processing system, the PLL having a reference clock input for receiv-

5   ing clock signals from a clock source, and a reset input for receiving a PLL reset signal

6   that resets the PLL

7   means for outputting a PLL reset signal to the PLL from a circuit having a clock

8   input to receive the clock signals and a reset input to receive a circuit reset signal;

9   means for generating a first timer signal at a first timer in response to receiving

10   the clock signals, and not generating the first timer signal in response to not receiving the

11   clock signals; and,

12   means for detecting the absence of the first timer signal at a second timer having

13   an input to receive the first timer signal, and in response ~~response~~ to detecting the ab-

14   sence of the first timer signal outputting the circuit reset signal to the circuit to enable the

15   circuit to reset the PLL circuit in the absence of the clock signals.

1   24. (Original) A computer readable media, comprising:

2   the computer readable media containing instructions for execution in a processor

3   for the practice of the method of claim 12.

1   25. (Currently amended) Electromagnetic signals propagating on a computer network,

2   comprising:

3   Tthe electromagnetic signals carrying instructions for the execution on a proces-

4   sor for the practice of the method of claim 12.